surface of the substrate may then be planarized utilizing conventional techniques such as chemical-mechanical polishing. The conductive material used to from the field plates may comprise a heavily doped polysilicon, a metal (or metal alloys), a silicide, or other suitable materials. In the completed device structure, field plate members **35***a* & **35***b* normally function as capacitive plates that may be used to deplete the extended drain region of charge when the HVFET is in the off state (i.e., when the drain is raised to a high voltage potential). In one embodiment, the lateral thickness of sidewall oxide **15** that separates each field plate **35** from sidewall **19** of mesa **14** is approximately 4 μm.

FIG. **1**D illustrates the example device structure of FIG. **1**C after masking of a top surface of the silicon substrate. In this example, the masking layer **21** comprises a layer of photoresist having openings **22***a* and **22***b* over oxide regions **15***a* and **15***b*, respectively, on opposite sides of mesa **14**. Note that the portion of masking layer **21** directly above mesa **14** extends or overlaps a distance "d" beyond the edge of sidewall **19** over each side of the mesa to cover first and second sidewall portions of oxide regions **15***a* and **15***b*. That is, the edge of each opening **22** closest to mesa **14** is not coincident with sidewall **19** of mesa **14**; rather, openings **22** are intentionally offset so that the nearest edge of each opening **22** is a small distance away from the corresponding mesa sidewall **19**. In one embodiment, the overlap distance "d" is approximately 0.2 μm to 0.5 μm.

FIG. **1**E illustrates the example device structure of FIG. **1**D after formation of the gate trenches **24***a* and **24***b*. Gate trenches **24***a* and **24***b* are formed by a first dielectric etch (shown by arrows **26**) that removes the dielectric material of oxide regions **15** in the areas directly below openings **22**. In one embodiment, the first dielectric etch is a plasma etch that is substantially anisotropic. First dielectric etch **26** is performed down to the desired or target depth, which is about 3 μm deep in one embodiment. A mixture of $C_4F_8$/CO/Ar/$O_2$ gases, for example, may be utilized for plasma etch **26**. Note that the anisotropic nature of the first etch produces a substantially vertical sidewall profile in the gate trench that does not extend or penetrate to the sidewalls **19** of mesa **14**. Stated differently, the overlap distance "d" of masking layer **21** is such that anisotropic etching through openings **22** does not attack the silicon mesa sidewalls **19**; instead, a portion of the dielectric material comprising oxide regions **15** still remains covering sidewalls **19** after the first dielectric etch.

FIG. **1**F illustrates the example device structure of FIG. **1**E following removal of the oxide covering the sidewalls **19** of mesa **14** in the gate trenches. A second dielectric etch (shown by arrows **29**) may performed through openings **22***a* & **22***b* of masking layer **21** to completely remove the remaining oxide on sidewalls **19***a* and **19***b*. In one embodiment, the second dielectric etch is a wet etch (e.g., using buffered HF) that is substantially isotropic in nature. The result is a pair of gate trench openings **27***a* and **27***b* that expose the epitaxial silicon material along sidewalls **19***a* & **19***b*, respectively, of mesa **14**.

In the embodiment shown, the second dielectric etch **29** is highly selective, which means that it etches the dielectric material at a much faster rate than it etches silicon. Using this process, the silicon surface of each sidewall **19** is undamaged, thereby allowing a high-quality gate oxide to be subsequently grown on the sidewall surface. In addition, due to the substantially isotropic nature of the second dielectric etch, the gate trench is etched at a similar rate in both the vertical and lateral directions. However, as the second dielectric etch is utilized to remove the remaining few tenths of a micron of silicon dioxide on the silicon mesa sidewall, the overall effect on the aspect ratio of trench gate openings **27** is relatively insignificant. In one embodiment, the lateral width of each gate trench opening **27** is approximately 1.5 μm wide, and the final depth is approximately 3.5 μm.

FIG. **1**G illustrates the example device structure of FIG. **1**F after removal of the masking layer **21**, formation of a high-quality, thin (e.g., ~500 Å) gate oxide layer **31**, which covers the exposed portions of sidewalls **19**, and subsequent filling of the gate trenches. In one embodiment, gate oxide layer **31** is thermally grown with a thickness in the range of 100 to 1000A. Masking layer **21** is removed prior to formation of gate oxide **31** .The remaining portion of each gate trench is filled with doped polysilicon or another suitable material, which form gate members **33***a* & **33***b* in the completed device structure.

FIG. **1**H illustrates the example device structure of FIG. **1**G in an expanded view that shows field plates **35***a* & **35***b* in relation to the trench gate structure. The trench gate structure includes gate members **33** disposed adjacent to, and insulated from, sidewalls **19** of mesa **14** by gate oxide layer **31**.

Practitioners in the art will appreciate that the overlap distance "d" of masking layer **21** should be sufficiently large enough such that even under a worst-case mask misalignment error scenario, the resulting overlap of masking layer **21** with respect to the sidewall of mesa **14** still prevents plasma etch **26** from attacking the silicon material along either one of sidewalls **19**. Similarly, the masking distance "d" of masking layer **21** should not be so large such that in a worst-case mask misalignment scenario the oxide remaining on either one of sidewalls **19** cannot be removed by a reasonable second dielectric etch. If, for example, the overlap distance "d" happens to be too large, the second dielectric etch **29** needed to remove the oxide covering sidewalls **19** might result in excessive thinning of the oxide remaining between (i.e., separating) gate members **33** and field plates **35**, potentially leading to inadequate isolation between these elements.

FIG. **1**I illustrates the example device structure of FIG. **1**H after formation of N+ source region **38** and P-type body region **39** near the top of epitaxial layer **12**. Source region **38** and body region **39** may each be formed using ordinary deposition, diffusion, and/or implantation processing techniques. After formation of the N+ source region **38**, the HVFET may be completed by forming source, drain, gate, and field plate electrodes that electrically connect to the respective regions/materials of the device using conventional fabrication methods (not shown in the figures for clarity reasons).

Although the present invention has been described in conjunction with specific embodiments, those of ordinary skill in the arts will appreciate that numerous modifications and alterations are well within the scope of the present invention. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

I claim:

**1**. A method comprising:

etching a semiconductor material of a first conductivity type to form first and second trenches that define a mesa having first and second sidewalls;

forming first and second dielectric layers respectively covering the first and second sidewalls;

forming, in a masking layer, first and second openings respectively disposed over the first and second dielectric regions on opposite sides of the mesa, the masking layer having a portion between the first and second openings that covers the mesa and overlaps a distance beyond each edge of the first and second sidewalls coincident with a top surface of the mesa;